REMARKS

Following entry of the present amendment, claims 50 through 93 are pending. In the Office Action mailed November 6, 2002, claims 50-61, were rejected under 35 U.S.C. §102(e) or, in the alternative, under 35 U.S.C. §103(a) over U.S. Patent No. 5,854,126 to Tobben (Tobben).

Reconsideration and withdrawal of the rejections are respectfully requested in view of the above amendments and the following remarks.

A. Rejection Under 35 U.S.C. §102(e) and 35 U.S.C. §103(a)

Independent claims 50 and 61 have been amended to recite limitations requiring that the cap layer has a uniform thickness which is sufficient to reduce reflectivity of light passing through such cap layer. This feature distinguishes claims 51 and 60 from Tobben because the cap layer of Tobben is of non-uniform thickness. Therefore, the cap layer of Tobben cannot function to reduce the reflectivity of light passing through the cap layer. In addition, independent claims 50 and 61 have been amended to require dielectric material to be deposited on surfaces exposed by the etching process including exposed surfaces of the cap layer, and that the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of depositing the dielectric material. Tobben neither discloses nor suggests a method of forming conducting structures in which a dielectric material is deposited on surfaces of the cap layer, and wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of depositing the dielectric material. Accordingly, Tobben can neither anticipate nor render obvious independent claims 50 and 61, as amended.

Therefore, Applicants submit that independent claims 50 and 61 are allowable over the cited references.

Dependent claims 51-60 and 62-79 depend from independent claims 50 and 61, respectively, and are allowable for at least the same reasons, and for the specific limitations recited therein. Applicants note that the Office Action mailed November 6, 2002, failed specifically to address the limitations embodied in the dependent claims. Should the Examiner maintain these

rejections, or issue new rejections against the claims, Applicants request that the Examiner specifically address each limitation embodied in the dependent claims.

B. New Claims 80-93

New claims 80-90 are based on previously pending claims 38-49, which were cancelled without prejudice or disclaimer in the Amendment After Final Office Action filed October 8, 2002. New claims 91-93 depend from independent claim 80.

1. Response to Paragraph 3 of Office Action mailed September 10, 2002.

In the Office Action mailed September 10, 2002, these claims were rejected under 35 U.S.C. §112, first paragraph. The Action asserted that the specification does not reasonably provide enablement for methods wherein the deposition step fails to substantially fill the gaps. Applicants traverse this rejection.

To support this rejection, the Action points to Fig. 4, and the fact that the drawing illustrates that the deposition/sputtering process deposits dielectric material to up to the level of layer 26.

First, as the Examiner apparently already appreciates, the "gaps" at this point in the process clearly extend to the top of layer 28, not layer 26, at least in those instances where layer 28 is left on after the etching of the conductive layer. Thus, the Examiner has clearly recognized that the scope of the limitation "substantially filled" (such as recited in allowed independent claim 59) is relatively broad, and does not require complete filling of the gap as it may exist at that time.

Nonetheless, as the Examiner can plainly discern from the specification, the "central objective" of the invention embodied in claim 42 is not so much to "substantially fill the gaps," but rather, to substantially fill a "high aspect ratio gap." See e.g., col. 8, ll. 62, which reads as follows:

> "....the HDPCVD step is carried out at a sufficiently high etch to deposition ratio so that the high aspect ratio gaps 36 between the wiring lines will be filled with oxide material."

Thus, after the high aspect ratio portion of the gap is filled, there is no need to continue a combined deposition/sputter process, and a conventional CVD can be performed. This is why the specification illustrates, for example in FIG. 4, that the high aspect ratio portion of gap 36 is filled in this way (layer 38), but the top portion of the gap 36 may be filled with a conventional CVD layer 40.

> "...the area above the deposited layer 38 may next be filled with layer 40...preferably the layer 40 is a PECVD oxide layer, which may be deposited at a higher speed than is typical of present HDPCVD processes."

In other words, a top portion of the high aspect ratio gap (to the extent any gap remains) may be filled with an additional dielectric layer. This points out that one key benefit conferred by the invention is that the "high aspect ratio" portion of the gap is substantially filled by a combined deposition/sputter operation, but the latter need not be continued past the point where a conventional CVD is then capable of completing the filling of the gap. Since a conventional CVD is faster in most cases, one skilled in the art can "tune" the process to achieve sufficient deposition coverage of high aspect ratio gaps while optimizing overall throughput. Stated another way, the "high aspect ratio gaps" between the metal lines can be filled with a combined deposition/sputter operation until the latter is not needed anymore, because the remainder of the gap can then be filled with a more conventional gap-filling technique.

2. Response to Paragraphs 4-6 of Office Action mailed September 10, 2002

The rejections in paragraphs 4-6 of the Office Action mailed September 10, 2002, concerned the use of the term "plasma based process...." which includes two separate components (deposition and etching) are also traversed.

First, the claim has been amended to recite that the plasma based process includes "... a deposition component and an adjustable etching component." This amendment is made not in response to any prior art, but because it more closely tracks the language of the specification.

As to the term "plasma based process", the specification clearly makes use of this terminology explicitly (.... [I]t should be recognized that any plasma based process can exhibit sputter etching and deposition mechanisms. When the present inventors discuss sputtering rates in HDPCVD processes, the present inventors intend to convey a sputtering rate in comparison to a base line level of sputtering characteristic of a process such as PECVD....). See e.g., page 8, lines 11-16, and implicitly. In the latter case the specification is replete with references to plasma based systems such as PECVD (plasma enhanced chemical vapor deposition), HDPCVD (high density plasma chemical vapor deposition), and provides a number of examples of sources for a plasma (ECR, inductively coupled plasma, helicons and electrostatically shielded radio frequency), and specific equipment vendors of plasma based systems. See e.g., page 6, line 28 through page 7, line 17. Third, as the Examiner well knows, this field of art contains numerous well known systems that utilize some form of a plasma to effectuate work on a substrate. For example, plasmas are used in the semiconductor art in deposition systems, sputtering systems, cleaning systems, and etching systems to name a few. Thus, the scope of the limitation "plasma based process" is well known to skilled artisans.

Consequently, the Applicants submit that this rejection is not well founded, as one skilled in the art would clearly understand and appreciate what is meant by the term "plasma based process," both from the specification, and from ordinary usage in this field of art.

Furthermore, as the Examiner will note, the specification provides extremely detailed explanations of how the plasma based process of the invention is not a generic PECVD process, but is in fact a particular type of plasma based process which uses both a deposition component and an adjustable etching component. The specification gives a specific example of a technique known at this time as HDPCVD as utilizing this type of approach. Nonetheless, as the Examiner will appreciate this terminology (HDPCVD) is simply a contemporary label for a type of system that uses these two types of components. The application is clearly broadly enabling to those skilled in the art to practice a variety of processes that employ a combination of these

types of components, regardless of what such process is called (HDPCVD or otherwise).

Consequently, applicants submit that new claims 80-90 comply with 35 U.S.C. § 112.

C. Conclusion.

All of the issues raised in the November 6, 2002 Office Action having been addressed, allowance of pending claims 50-93 is respectfully requested.

A petition for a one-month extension of time is enclosed. The enclosed check for $ 470 is intended to cover the one-month extension of time ($110) and the fee for adding twenty dependent claims ($360). However, the Office is authorized to charge any fee deficiency associated herewith to Deposit Account No. 50-1123. Please contact the undersigned by telephone should any issues remain.

Respectfully submitted,

March 6, 2003

Jed Caven, Reg. No. 40,551
HOGAN & HARTSON
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(303) 454-2432 Tel
(303) 899-7333 Fax

MARKED UP COPY OF AMENDED CLAIMS

Please amend claims 50 and 61 as follows:

50. (Amended) A method for forming conducting structures separated by gaps on substrate comprising:

providing a substrate and a wiring line layer above the substrate;

forming a cap layer above the wiring line layer, wherein said cap layer has a uniform thickness which is sufficient to reduce reflectivity of light passing through such cap layer;

etching through a portion of the cap layer and portions of the wiring line layer to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material on surfaces exposed by the etching process including exposed surfaces of the cap layer to substantially fill the gaps between the wiring lines, said dielectric material including a layer formed by high density plasma chemical vapor deposition,

wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of depositing the dielectric material.

61. (Amended) A method of forming conducting structures separated by gaps filled with dielectric material, comprising the steps of:

providing a substrate containing silicon, the substrate having a surface;

forming a surface layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy, the surface layer disposed on the substrate surface.

forming a metal wiring layer on the surface layer, the metal wiring layer having an upper surface;

forming a protective layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy, the protective layer disposed on the upper surface of the metal wiring layer, the protective layer having a top surface;;

forming a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, a silicon–rich oxide, and an oxynitride,

the cap layer disposed on the top surface of the protective layer, wherein said cap layer has a uniform thickness which is sufficient to reduce reflectivity of light passing through such cap layer;

forming a patterned photoresist layer above the cap layer, said patterned photoresist layer covering selected portions of the cap layer and exposing other portions of the cap layer;

etching the cap layer, the protective layer and the metal wiring layer to form the conductive structures separated by gaps; and

forming a layer of high density plasma chemical vapor deposition (HDPCVD) dielectric material on surfaces exposed by the etching process including exposed surfaces of the cap layer, [within the gaps]

wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of depositing a dielectric material on surfaces exposed by the etching process.

Please add new claims 62-93 as follows:

62. (New) The method of claim 61, wherein the cap layer is used as a hard mask during etching of the wiring line layer.

63. (New) The method of claim 61, wherein portions of the cap layer are partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

64. (New) The method of claim 61, wherein the cap layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, or oxynitride.

65. (New) The method of claim 61, wherein the layer of dielectric material formed by HDPCVD substantially fills the gaps between the conductive structures.

66. (New) The method of claim 61, wherein the layer of dielectric material formed by HDPCVD is deposited onto a surface of the substrate, onto side surfaces of the metal wiring layer, the surface layer, the protective layer, and the cap layer.

67. (New) The method of claim 61, wherein the layer of dielectric material formed by HDPCVD is deposited onto an upper surface of the cap layer.

68. (New) The method of claim 61, further comprising removing the patterned photoresist layer prior to forming a layer of high density plasma chemical vapor deposition (HDPCVD) dielectric material.

69. (New) The method of claim 61, wherein the cap layer protects the underlying wiring layer during the process of forming a layer of high density plasma chemical vapor deposition (HDPCVD) dielectric material.

70. (New) The method of claim 61, wherein the protective layer comprises a material having a first dielectric constant and the antireflective coating comprises a material having a second dielectric constant, different from the first dielectric constant.

71. (New) The method of claim 61, wherein the first dielectric constant and the second dielectric constant form a graded index of refraction.

72. (New) The method of claim 71, wherein the graded index of refraction reduces boundary reflections between the cap layer and the first antireflective coating.

73. (New) The method of claim 61, wherein the antireflective coating of the cap layer reduces reflection by generating destructive interference in reflected light.

74. (New) The method of claim 61, wherein twice the thickness of the cap layer is an odd number of the wavelengths of the exposure light, compensating for the dielectric constant of the cap layer.

75. (New) The method of claim 50, wherein the protective layer comprises a material having a first dielectric constant and the antireflective coating comprises a material having a second dielectric constant, different from the first dielectric constant.

76. (New) The method of claim 50, wherein the first dielectric constant and the second dielectric constant form a graded index of refraction.

77. (New) The method of claim 76, wherein the graded index of refraction reduces boundary reflections between the cap layer and the first antireflective coating.

78. (New) The method of claim 50, wherein the antireflective coating of the cap layer reduces reflection by generating destructive interference in reflected light.

79. (New) The method of claim 61, wherein twice the thickness of the cap layer is an odd number of the wavelengths of the exposure light, compensating for the dielectric constant of the cap layer.

80. (New) A method for forming conducting structures separated by gaps on a substrate comprising:

providing a substrate and a wiring line layer above the substrate;

forming a first antireflective coating above the wiring line layer;

forming a cap layer adapted for protecting the wiring line layer during a plasma based process, the cap layer being situated above the first antireflective coating, wherein the cap layer and the first antireflective coating have different dielectric constants;

etching through portions of the first antireflective coating, a portion of the cap layer and a portion of the wiring line layer to form wiring lines separated by high aspect ratio gaps; and

depositing a dielectric material to substantially fill said gaps, including using a first plasma based process having both a deposition component and an adjustable etching component at least until any high aspect ratio gaps are substantially filled, followed by a second plasma based process that fills any remaining portion of said gaps and results in a planarized surface, and which second plasma based process does not include an adjustable etching component.

81. (New) The method of claim 80, wherein the first antireflective coating absorbs portions of radiation applied during a lithographic process

and the cap layer creates destructive interference with portions of radiation applied during the lithographic process.

82. (New) The method of claim 80, wherein the cap layer cap layer also functions as a mask during the etching process.

83. (New) The method of claim 80, wherein an additional portion of the cap layer is etched while the cap layer protects the wiring line layer during the plasma based process.

84. (New) The method of claim 80, further comprising forming a surface layer between the substrate and the wiring line layer.

85. (New) The method of claim 80, further comprising the step of removing the cap layer before depositing a dielectric material within the gaps.

86. (New) The method of claim 80, wherein portions of the cap layer are removed and portions of the cap layer act as a mask during the etching of the first antireflective coating and the wiring line layer.

87. (New) The method of claim 80, wherein after etching each wiring line has a portion of the cap layer thereon, the portion of a cap layer on each wiring line having a cross-sectional shape selected from the group consisting of a rectangle, a triangle, trapezoid, and a rectangle having its upper corners etched away.

88. (New) The method of claim 80 wherein the cap layer and the first antireflective coating are used as a hard mask.

89. (New) The method of claim 80 wherein the cap layer and the first antireflective coating form a graded change in an index of refraction.

90. (New) The method of claim 80 wherein the cap layer has a dielectric constant that is closer than a dielectric constant of the first antireflective coating to a subsequent photoresist mask layer dielectric constant.

91. (New) The method of claim 80, wherein the second plasma based process deposits material at a higher rate than the first plasma based process.

92. (New) The method of claim 80, wherein the second plasma based process is a PECVD oxide process.

93. (New) The method of claim 80, wherein the cap layer comprises silicon, oxygen, and nitrogen.